

REMARKS

Claims 1, 3, 4, 6 to 16 and 20 to 29 remain pending in the application, with claims 1, 4, 7, 11 and 14 being the independent claims. Reconsideration and further examination are respectfully requested.

In the Office Action, claims 1, 4, 6, 7, 9 to 12, 14 to 16 and 20 to 29 were rejected under 35 U.S.C. § 102(b) over Japanese Patent JP815057 (Tarasawa); and claims 3, 8 and 13 were rejected under §103(a) over Tarasawa. Withdrawal of these rejections is respectfully requested for the following reasons.

As set forth in detail in previous Responses, the present invention concerns circuits and techniques for cancelling electromagnetic or environmental noise. The cited reference, Tarasawa, appears to disclose a related noise-cancellation circuit. However, in many respects, the present invention is different than the circuit disclosed in Tarasawa.

In order to simplify the present remarks, the following discussion will emphasize certain features and limitations of the present invention. While the emphasized features are believed to be very relevant to the present rejections, it should be understood that the present invention is defined by the combination of all of the features recited in each individual claim. In each case, the recited combination of features is believed to be novel and non-obvious over the applied art. However, given the long prosecution history of this case, it is assumed that the Examiner is quite familiar with the present

Serial No.: 08/840,947

invention and, therefore, a reiteration of each individual feature and limitation is not believed to be necessary in the present case.

Initially, it appears that the Examiner is reading the "first circuit" and the "second circuit" (as such terms are recited in some of the pending claims) on Tarasawa's first delta-sigma modulation circuit 2 and second delta-sigma modulation circuit 3, respectively. This assumption forms the basis for the remainder of these remarks.

Claims 1, 3, 4, 6, 9, 10 and 20 to 26 recite (either directly or through their dependencies) the feature of a digital circuit located proximate to the first and second circuits. In the Office Action, it appears that the Examiner is reading this limitation on Tarasawa's circuit elements 15 and 25. However, a careful analysis of Tarasawa's first and third figures indicates that element 15 actually is part of delta-sigma converter 2 and element 25 is part of delta-sigma converter 3. As sub-components of such convertors, elements 15 and 25 could not be said to be proximate to them. Lacking this limitation of the subject claims, Tarasawa could not have anticipated such claims.

Claims 4, 6, 14 to 16, 25, 26 and 29 (either directly or through their dependencies) include the feature that the output of the second circuit that is based on its input signal is a null output. Nothing in Tarasawa is seen to disclose this feature of the invention, and the Office Action has not even alleged that it does. Accordingly, for at least this reason, the subject claims could not have been anticipated by Tarasawa.

Claims 6 and 10 recite the additional feature that the first circuit, the second circuit, the third circuit and the digital circuit are on a single integrated circuit chip.

Serial No.: 08/840,947

Tarasawa does not appear to disclose this feature of the invention, and the Office Action has not even alleged that it does. Accordingly, for at least this additional reason, the subject claims could not have been anticipated by Tarasawa.

Claims 7 to 10 and 27 (either directly or through their dependencies) recite the feature of supplying to the input of the second circuit an inverse of the signal provided to the input of the first circuit. Tarasawa does not appear to disclose this feature of the invention, and the Office Action has not even alleged that it does. Accordingly, for at least this reason the subject claims could not have been anticipated by Tarasawa.

Claim 11 and its dependent claims 12, 13 and 28 recite the features of: a plurality of analog circuits, a noise separator circuit that is proximal to the plurality of analog circuits and produces a noise signal which is approximately equal to the noise component of the signal output by each of the plurality of analog circuits, and a noise cancelling circuit which processes the output signals with the noise signal to reduce the noise component of the signal output by each of the plurality of analog circuits.

Tarasawa, on the other hand, appears merely to disclose first and second delta-sigma modulation circuits 2 and 3. Even assuming that such circuits constitute the recited plurality of analog circuits (on which Applicant does not take a position), Tarasawa still would fail to disclose any noise separator circuit that is proximal to such plurality of analog circuits and produces a noise signal that is approximately equal to the noise components of the signal output by each of such plurality of analog circuits, much less

Serial No.: 08/840,947

the other recited limitations which follow this limitation. Accordingly, for at least this reason, Tarasawa could not have anticipated the present claims.

As indicated above, many of the claim limitations are not disclosed by Tarasawa, and in many cases, there is not even an allegation that such limitations are disclosed. Moreover, each of the pending claims recites at least one of such limitations.

Thus, in view of the foregoing remarks, all of the claims in the application are believed to be in condition for allowance, and an indication to that effect is respectfully requested.

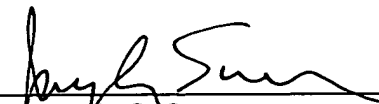
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Respectfully submitted,

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Dated: April 18, 2003

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